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EXAMINER	
SONG, MATTHEW J	

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 03/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/904,131	UEDA, TETSUZO	
	Examiner	Art Unit	
	Matthew J Song	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/8/2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-17 and 19-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-17 and 19-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/3/2003 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 11 and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by Purdes (US 4,830,984).

Purdes discloses a layer of a tensioning material on the bottom or second side of silicon substrate to counteract the tensioning force and warping effect brought on by a gallium arsenide layer applied to the first or top side of the silicon substrate (col 2, ln 55-67). Purdes also teaches

reducing or eliminating warpage arising from formation of a gallium arsenide layer on a silicon substrate (col 2, ln 25-35). Purdes also teaches it is within the scope of the present invention that the layer formed on the first surface of the silicon substrate may comprise other materials other than gallium arsenide (col 5, ln 35-50) and the substrate may comprise other materials other than silicon (col 8, ln 5-20). Purdes also discloses after the layer of tensioning material is formed on the backside of the silicon substrate and treated to produce the desired warping effect by annealing at 1000°C, the gallium arsenide layer may be formed after cooling to 650°C (col 5, ln 10-25), this reads on applicant's heating step and the layered substrate exhibits bowing after being cooled down from the heating step. Purdes teaches different thermal expansion coefficients (claim 2, 3, and 7).

Referring to claim 11, Purdes teaches after the layer of tensioning material is formed on the backside of the silicon substrate and treated to produce the desired warping effect by annealing at 1000°C, this reads on applicant's layered substrate which exhibits bowing. And Purdes teaches after an epitaxial gallium arsenide is formed and cooled, the structure will have a planar form (claim 1 and col 3, ln 35-65), this reads on applicant's so as to reduce bowing.

4. Claims 11 and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by Chen et al (US 5,562,770).

Chen et al discloses a substrate **140** having a device layer **150** at the top and another layer of film **160** at the bottom of the substrate **140** and a substrate, which is flat when the layer **160** has negligible intrinsic stress (col 5, ln 40-67 and Fig 7A), this reads on applicant's growing an epitaxial layer on a layer substrate to reduce bowing. Chen et al also teaches

providing a substrate, processing the backside of the substrate by depositing an insulating film so as to impart a convex curvature to the frontside of the substrate and growing an epitaxial layer on the substrate (claim 10 and 12). Chen et al also teaches the other applications, such as III-V compound device may be used with the instant invention (col 7, ln 1-25). Chen et al also teaches the thin film on the back surface determines the magnitude and direction of the net stress and determines if the substrate is convex or concave (col 5, ln 65 to col 6, ln 5). Chen et al also teaches minimizing the concavity of the substrate (col 6, ln 55-65). Chen et also teaches the calculation of film thickness, film stress, wafer thickness and wafer bow given the values of the other are well known (col 8, ln 1-10). Chen et al also teaches imparting a convex structure to the substrate by removing layers of a thin film or adding thin film layers to the backside of the substrate (Abstract).

Referring to claim 11, Chen et al teaches a silicon substrate and an insulating layer of silicon oxide, silicon nitride or low temperature oxide (col 6, ln 5-15,50-60). Silicon and the insulating layer inherently have different thermal coefficients of expansion.

Referring to claim 26, Chen et al teaches thermally grown layers and a curvature and the substrate is convex or concave prior to substrate processing operations such as grinding, this reads on applicant's layered substrate include heating and exhibits bowing after cooling.

5. Claims 11, 13, 14, and 24-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Molnar (US 6,086,673) in view of Purdes (US 4,830,984) or Chen et al (US 5,562,770).

Molnar discloses growing an III-V nitride epitaxial layer on a foreign substrate, where the foreign substrate which can be employed includes sapphire, spinel, silicon carbide, silicon, YAG,

GGG, gallium arsenide, titanium nitride, titanium carbide, ScN, InN, AlN, $In_xGa_yAl_{1-x-y}As$, $In_xGa_yAl_{1-x-y}$ or $In_xGa_yAl_{1-x-y}N$, where $0\leq x\leq 1$, $0\leq y\leq 1$,and $0\leq x+y\leq 1$. Molnar also discloses the growth substrate can also consist of layered structures composed of combinations of these materials and other such materials (col 7, ln 1-20 and Abstract). Molnar also disclose the substrate can be removed from a GaN epitaxial layer by etching, electrochemical polishing or by other suitable processes (col 11, ln 25-40). Molnar also discloses a growth temperature of 800-1250°C for GaN deposition (col 9, ln 20-30) and cooling the substrate after deposition at a rate of 1°C/min to 200°C/min under a NH_3 atmosphere (col 11, ln 15-30)

Molnar is silent to the thermal coefficients of the substrate materials, however this is inherent to Molnar because the different materials of a layered substrate, such as sapphire and GaN ($In_xGa_yAl_{1-x-y}N$, where x=0 and y=1), inherently have different thermal coefficients. Also, applicant's admission teaches a thermal mismatch between GaN and sapphire (pg 3, ln 1-15).

Molnar is also silent to the layered substrate exhibits bowing. However, this is inherent to Molnar because Molnar discloses a layered substrate of SiC and sapphire, as applicant, note instant claim 13. Also, Applicant's admission teaches a layered substrate, where the bowing of a GaN/ sapphire substrate occurs for a GaN thickness of greater than 0 microns (Fig 1C).

Molnar is also silent to growing an epitaxial layer on a layered substrate so as to reduce bowing.

In a method of forming a planar structure, note entire reference, Purdes teaches a layer of a tensioning material on the bottom or second side of silicon substrate to counteract the tensioning force and warping effect brought on by a gallium arsenide layer applied to the first or top side of the silicon substrate (col 2, ln 55-67). Purdes also teaches reducing or eliminating

warpage arising from formation of a gallium arsenide layer on a silicon substrate (col 2, ln 25-35). Purdes also teaches it is within the scope of the present invention that the layer formed on the first surface of the silicon substrate may comprise other materials other than gallium arsenide (col 5, ln 35-50) and the substrate may comprise other materials other than silicon (col 8, ln 5-20). Purdes also teaches after the layer of tensioning material is formed on the backside of the silicon substrate and treated to produce the desired warping effect by annealing at 1000°C, the gallium arsenide layer may be formed after cooling to 650°C (col 5, ln 10-25), this reads on applicant's heating step and the layered substrate exhibits bowing after being cooled down from the heating step. Purdes teaches different thermal expansion coefficients (claim 2, 3, and 7).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the layered structure of materials with different thermal conductivities taught by Molnar with Purdes' method of reducing warpage by depositing an epitaxial layer, which counteracts a tensioning force (claim 1) to form a desirable planar structure (claim 14).

In a method of epitaxially growing a device layer (Abstract), Chen et al teaches a substrate **140** having a device layer **150** at the top and another layer of film **160** at the bottom of the substrate **140** and a substrate, which is flat when the layer **160** has negligible intrinsic stress (col 5, ln 40-67 and Fig 7A), this reads on applicant's growing an epitaxial layer on a layer substrate to reduce bowing. Chen et al also teaches providing a substrate, processing the backside of the substrate by depositing an insulating film so as to impart a convex curvature to the frontside of the substrate and growing an epitaxial layer on the substrate (claim 10 and 12). Chen et al also teaches the other applications, such as III-V compound device may be used with the instant invention (col 7, ln 1-25). Chen et al also teaches the thin film on the back surface

determines the magnitude and direction of the net stress and determines if the substrate is convex or concave (col 5, ln 65 to col 6, ln 5). Chen et al also teaches minimizing the concavity of the substrate (col 6, ln 55-65). Chen et also teaches the calculation of film thickness, film stress, wafer thickness and wafer bow given the values of the other are well known (col 8, ln 1-10). Chen et al also teaches imparting a convex structure to the substrate by removing layers of a thin film or adding thin film layers to the backside of the substrate (Abstract).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the layered structure of materials with different thermal conductivities taught by Molnar with Chen's method of wafer curvature manipulation (col 8, ln 40-50) to minimize dislocation motion and multiplication in a device layer (col 7, ln 1-25).

Referring to claim 13-14, the combination of Molnar and Chen or the combination of Molnar and Purdes teaches an III-V nitride epitaxial layer and a substrate of a layered structure of Sapphire and silicon, sapphire and an III-V nitride, sapphire and ZnO, and sapphire and SiC.

Referring to claim 24, the combination of Molnar and Chen or the combination of Molnar and Purdes teaches removing the substrate ('673 col 11, ln 25-40).

Referring to claim 25, the combination of Molnar and Chen or the combination of Molnar and Purdes teaches electrochemical polishing, this reads on applicant's mechanical polishing.

Referring to claim 26, the combination of Molnar and Chen or the combination of Molnar and Purdes teaches a layered substrate of GaN and sapphire. Molnar also discloses forming a GaN layer on a sapphire substrate at a temperature between 800 and 1250°C and cooling at a rate of 1-200°C/min, the combination of Molnar and Chen or the combination of Molnar and Purdes is silent to the layered substrate exhibits bowing after being cooled down, however this is

inherent to the combination of Molnar and Chen or the combination of Molnar and Purdes because the combination of Molnar and Chen or the combination of Molnar and Purdes discloses similar layers, as applicant, which have different coefficients of thermal expansion and the combination of Molnar and Chen or the combination of Molnar and Purdes discloses cooling the substrate, as applicant. Furthermore, the amount of bowing can be determined using the teachings of Olsen et al ("Calculated stresses in multilayered heteroepitaxial structures") below.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Molnar (US 6,086,673) in view of Purdes (US 4,830,984) or Chen et al (US 5,562,770) as applied to claims 11, 13, 14, 24-26 and 28 above, and further in view of Zheleva et al (WO 99/65068).

The combination of Molnar and Chen or the combination of Molnar and Purdes discloses all of the limitations of claim 12 including the deposition of an epitaxial gallium nitride layer, as discussed previously, except the step of selective etching a portion of the epitaxial layer.

In a method of forming improved gallium nitride layers, note entire reference, Zheleva et al teaches an underlying gallium nitride layer **104** is grown on a SiC substrate **102** and the underlying gallium nitride layer includes a plurality of sidewalls **105** (pg 5, ln 10-35). Zheleva et

al also teaches the posts **106** and trenches **107** that define the sidewalls **105** may be fabricated by selective etching (pg 6, ln 1-5). Zheleva et al also teaches the sidewalls **05** of the gallium nitride layer are laterally grown to from a lateral gallium nitride layer **108a** in the trench **107**. It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Molnar and Chen or the combination of Molnar and Purdes with Zheleva et al's selective etching of GaN to form a trench which can be used to form a relatively defect free GaN semiconductor layer (pg 2, ln 15-20).

8. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Molnar (US 6,086,673) in view of Purdes (US 4,830,984) or Chen et al (US 5,562,770) as applied to claims 11, 13, 14, 24-26 and 28 above, and further in view of Kito et al (US 6,110,279).

The combination of Molnar and Chen or the combination of Molnar and Purdes discloses all of the limitations of claim 25, as discussed previously. However, if there is an art recognized difference between electrochemical polishing and mechanical polish and electrochemical polishing does not read on mechanical polishing; then it would be obvious in view of Kito et al.

In a method of producing a single crystal, note entire reference, Kito et al teaches forming a SiC single crystal layer **15** on a Silicon wafer **14** and removing the silicon wafer by a chemical technique whereby only the SiC layer remains. Kito et al also teaches a mechanical polishing step may be employed instead of the chemical technique (col 45-60). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Molnar and Chen or the combination of Molnar and Purdes with Kito et al's

method of removing a substrate using mechanical polishing because substitution of known equivalents for the same purpose is held to be obvious (MPEP 2144.06).

9. Claims 15-16, 19-21, and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hansson (DE 198 47 101), where US 6,316,361 is used an accurate translation or Hansson (US 6,316,361) in view of Westmoreland (US 5,227,331).

Hansson discloses placing a semiconductor wafer in a CVD reactor **1** having an upper reaction chamber **2**, a lower reactor chamber **3** and a dividing wall **4** and a holding ring **6**, heating the semiconductor wafer and depositing a layer on the back of the wafer and simultaneously depositing an epitaxial layer on the front and the back of the wafer by feeding various process gases into the two reactor chambers (col 3, ln 1-67, col 4,ln 30-65 and Fig 2 of '361). Hansson discloses an advantage is that epitaxial layers can be deposited simultaneously on both sides of a wafer using only one CVD reactor (col 2, ln 25-65 of '361). Hansson also discloses a polysilicon layer can be deposited on the back of the wafer (col 3, ln 11-16 of '361). Hansson also discloses while at least one epitaxial layer is being deposited on the front of the wafer in the upper reactor, the lower reactor is flushed with inert flushing gas (col 3, ln 25-33 of '361). Hansson also discloses a feed lines **11** and **13** and forming a protective layer on the backside of the wafer and forming an epitaxial layer on the front side (Claim 1). Hansson also discloses heat sources **15** located on the exterior of the chamber (Fig 2). Hansson discloses the process gases for an epitaxial layer are well known and trichlorsilane is preferable (col 3, ln 20-35). Hansson also discloses the protective layer of $Si_xN_yH_z$, the process gases for an epitaxial

layer using trichlorosilane and $Si_xN_yH_z$ are inherently different. The process gases used for $Si_xN_yH_z$, reads on applicants another set of reactant species.

Hansson does not disclose directly heating the substrate by a radiation source with using any heat sink material.

In an improved CVD method for semiconductor manufacturing, note entire reference, Westmoreland teaches a heat source uses radiant energy to heat a semiconductor structure, where tungsten halogen lamps and graphite heaters are suitable (col 2, ln 50-60). Westmoreland also teaches the heat source can be located within the reaction chamber of the CVD reactor, this reads on applicant's directly heating by a reaction source without using any heat sink material because the radiation means is located inside the chamber rather than outside the chamber and the heat source is shown to act directly on a substrate (Fig 1B). Westmoreland also teaches the heat source is preferably directed at the semiconductor structure for instantaneously increasing the surface temperature thereof (col 5, ln 1-55).

It is well known in the art that direct heating of a substrate is preferable because it can control the temperature of a substrate more precisely and the use of a susceptor is not desirable because of long heating times, as evidenced by Hirai et al (US 4,312,921) and Habuka (US 5,913,974) below. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Hansson with Westmoreland's heat source located within the reaction chamber to control the temperature of the substrate more precisely and increase productivity.

Referring to claim 19, the combination of Hansson and Westmoreland teaches a holding ring **6**, this reads on applicant's placing a substrate in a system so that each side of the substrate

is not completely covered by any parts or susceptor blocks, and a dividing wall, this reads on applicant's preventing mixing of the two sets of reactant gases and a heating means located within the chamber, this reads on applicant's without using any heat sink materials.

Referring to claims 20 and 27, the combination of Hansson and Westmoreland teaches a dividing wall **4**, this reads on applicant's physical partition.

Referring to claim 21, the combination of Hansson and Westmoreland teaches inert flushing gases, this reads on applicant's inert gas flows.

10. Claims 17 and 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hansson (DE 198 47 101), where US 6,316,361 is used an accurate translation, or Hansson (US 6,316,361) in view of Westmoreland (US 5,227,331) as applied to claims 15-16, 18-21, 27 and 29-30 above, and further in view of Manabe et al (US 5,620,557).

The combination of Hansson and Westmoreland teach all of the limitations of claim 22, as discussed previously, except both sets of reactant species comprise a nitrogen source and a group III metal source.

In a method of making a semiconductor, Manabe et al discloses a sapphire substrate **1**, intermediate ZnO layers **2a, 2b**, on the sapphire substrate and forming GaN layers **3a, 3b** by Metal organic vapor phase epitaxy on the intermediate ZnO layers (col 2, ln 55 to col 3, ln 19). Manabe et al also discloses GaN layers are formed by releasing reactant gases of ammonia, a nitrogen source, and trimethyl gallium, a group III metal source, over both surfaces of the sapphire substrate (col 3, ln 15-24). Manabe et al also teaches other III-V nitrides, $Al_xGa_yIn_{1-x-}$

$_yN$, can be formed (claim 1). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Hansson and Westmoreland with Manabe et al to form gallium nitride, which is a useful compound semiconductor for light emitting diodes (col 1, ln 10-26).

Referring to claim 23, the combination of Hansson, Westmoreland and Manabe et al teaches supplying nitrogen and a group III metal and forming a polysilicon protective layer on the back side using trichlorosilane (col 3, ln 25-30).

Response to Arguments

11. Applicant's arguments with respect to claims 11-17 and 19-27 have been considered but are moot in view of the new ground(s) of rejection.

12. Applicant's arguments filed 11/3/2003 have been fully considered but they are not persuasive.

Applicant's argument that there is no objective evidence from the prior art that suggest the desirability of direct heating is noted but is not found persuasive based on the new grounds of rejection. The motivation to combination Hansson with Westmoreland has been changed. The new motivation incorporates the desirability to use direct heating is well known in the art, as evidenced by Habuka (US 5,913,974) and Hirai et al (US 4,312,921). Therefore, applicant's argument that there is no specific teaching of direct heating is desirable is moot.

Applicant's argument that Molnar teaches away from direct heating is noted but is not found persuasive. Molnar merely suggest other methods and does not teach using a direct heating

does not constitute a teaching away. Disclosed examples and preferred embodiments do not constitute a teaching away from a broader disclosure or non-preferred embodiments (MPEP 2123). Furthermore, Molnar is not incorporated into the rejection. The rejection is based on the teachings of Hansson and Westmoreland and does not include Molnar.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Solomon (US 5,919,305) teaches substrate removal using etching or polishing away after an epitaxial layer is formed and the motivation is to reduce optical absorption or reduce resistive heating in the epitaxial layer by providing a better heat sink directly to the epitaxial layer (col 1 and col 2).

Lee et al (US 4,835,116) teaches III-V/Si and III-V/(Ge/Si) wafers exhibit warping due to thermal strain (col 4, ln 20-30).

Sugawara et al (US 6,232,137) teaches the thickness of layers is critical in terms of generation of crystallographic defects caused by lattice mismatch between layers (col 2, ln 60 to col 3, ln 10).

Sugawara et al (JP 10-335700) is a 102(b) equivalent to US 6,232,137.

Olsen et al ("Calculated Stresses in multilayered heteroepitaxial structures") teaches a method of calculation stress in multilayered structures, note entire reference.

Hirai et al (US 4,312,921) teaches the heating of a substrate using direct heating by an electric resistance heating, high frequency heating and the like is preferable to indirect heating because the temperature of the substrate can be controlled more precisely (col 11, ln 1-15).

Habuka (US 5,913,974) teaches heating of a semiconductor substrate uniformly over an entire area by directly heating with radiant light emitted from infrared lamps without using a susceptor reduces the time required to reach a desired temperature (col 1, ln 10-55).

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew J Song whose telephone number is 571-272-1468. The examiner can normally be reached on M-F 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571-272-1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Matthew J Song
Examiner
Art Unit 1765

MJS

NADINE G. NORTON
SUPERVISORY PATENT EXAMINER